



PULSED DYNAMIC KEEPER GATING

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BACKGROUND

Field of the Invention

[1001] This invention relates to dynamic circuits and more particularly to keeper devices utilized in dynamic circuits.

Description of the Related Art

[1002] Dynamic Complementary Metal Oxide Semiconductor (CMOS) circuits precharge a node and conditionally discharge the node based on inputs evaluated by the circuit. Referring to FIG. 1, a prior art OR circuit 100 is illustrated with a p-channel precharge device 102 and n-channel evaluation logic. The n-channel evaluation logic includes devices 104-108 and an n-channel ground switch 110. Devices 102 and 110 are enabled during opposite phases of the signal CLOCK, disabling at least one transistor in the path between VDD and VSS at a given time. Therefore, a DC current path does not exist from VDD to VSS and the steady-state current is zero. However, a static leakage current exists due to reverse bias leakage between diffusion regions and the substrate in the n-channel devices 104-110. This leakage current may sufficiently discharge dynamic node 116 to produce an incorrect value at the output node, OUT.

[1003] The effects of this leakage current may be countered by introducing keeper 112 at dynamic node 116. Keeper 112 latches the output of the circuit. Alternatively, keeper 112 could be statically configured by grounding the gate input. Keeper 112 is a weak keeper, that is, a p-transistor designed to have a low gain achieved by a small W/L ratio so that the gain is low enough to be overcome by pull-down transistors 104-

110. However, keeper 112 has a large enough gain to offset the effects of the leakage current. In circuits with a large number of inputs, each input requiring a pull-down transistor coupled to a single dynamic node, the leakage current may be too large for a weak keeper to counteract. Replacing the weak keeper of keeper 112 with a strong keeper (i.e., a device that has a high gain achieved by a large W/L ratio), slows down circuit transitions due to the additional capacitance of the stronger keeper transistor. In addition, pull-down devices may be unable overcome the strong keeper transistor and the dynamic node may not switch properly, resulting in the circuit producing incorrect output values at the output node. Instead, prior art circuits typically maintain proper functionality and high speed by limiting the number of pull-down transistors used with a weak keeper. The limit on the number of pull-down transistors may limit the number of inputs the dynamic circuit can evaluate. For example, in FIG. 1, circuit 100 is limited to k input pull-down devices. As a result, circuit designs using these dynamic circuits may implement more complex circuitry to achieve the same functionality as a device having a greater number of input pull-down devices. Increasing circuit complexity may decrease speed, increase circuit size, and increase manufacturing costs.

[1004] Therefore, it would be desirable to use a strong keeper to overcome leakage of the evaluation devices of a large number of inputs, without compromising the functionality or speed of the circuit.

SUMMARY

[1005] Accordingly, it has been discovered that a keeper circuit for a dynamic node of a circuit may be designed or configured such that the effective strength of the keeper circuit operating on the dynamic node may be reduced during an interval in which at least one path of an evaluation circuit is sensitive to a strong keeper device. This sensitivity may otherwise produce incorrect functionality and/or reduced speed of a circuit with a keeper device.

[1006] In one embodiment in accordance with the present invention, a circuit includes a dynamic node, an evaluation circuit, and a keeper circuit coupled to the dynamic node. The circuit may include a precharge device. The precharge device and the evaluation circuit may operate during different phases of a control signal. The

keeper circuit may latch the circuit output. The keeper circuit includes a keeper gating device coupled to a keeper device. In one realization, the keeper circuit includes a weak keeper device. The keeper circuit is responsive to a keeper control. The keeper control may be clocked. The keeper control may be self-timed. The keeper device may be sized to sufficiently overcome leakage current in the evaluation circuit. The weak keeper device may be minimally sized to sufficiently overcome noise while the keeper device is effectively disabled.

[1007] In one embodiment in accordance with the present invention, the reduction in the effective strength of the keeper circuit occurs before arrival of the fastest signal coupled to a sensitive output path of the evaluation circuit. The effective keeper circuit strength is restored after arrival of the slowest signal coupled to the sensitive output path of the evaluation circuit.

[1008] In one embodiment in accordance with the present invention, the dynamic node is precharged high. The evaluation circuit may be n-logic. In one embodiment in accordance with the present invention, the dynamic node is precharged low. The evaluation circuit may be p-logic.

[1009] In another embodiment in accordance with the present invention, a method for evaluating a dynamic node is provided. The dynamic node is precharged, a keeper coupled to the dynamic node is effectively disabled during an interval in which at least one path in an evaluation circuit is sensitive to a keeper device, an evaluation circuit is evaluated, and the keeper device is effectively enabled. The dynamic node may be protected from noise during the disabling of the keeper device.

[1010] In another embodiment in accordance with the present invention, a method for reducing effective keeper circuit strength during an interval in which at least one path of an evaluation circuit is sensitive to a strong keeper device is provided. A weak keeper device may remain effective during the interval.

BRIEF DESCRIPTION OF THE DRAWINGS

[1011] The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

[1012] **FIG. 1** is a prior art implementation of an OR circuit.

[1013] **FIG. 2** illustrates an exemplary OR circuit configured consistent with the present invention.

[1014] **FIG. 3** illustrates a timing diagram consistent with the present invention.

[1015] **FIG. 4** illustrates another exemplary OR circuit configured consistent with the present invention.

[1016] The use of the same reference symbols in different drawings indicates similar or identical items.

DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

[1017] Referring to FIG. 2, circuit 200 includes keeper 212 in series with keeper gating device 218. Keeper 212 is a p-transistor designed to have a gain sufficient to offset the effects of leakage currents in evaluation circuits with a large number of pull-down devices. The size of keeper 212 may be determined by simulating circuit 200 and determining the W/L ratio of keeper 212 necessary to achieve the appropriate gain, or by any other method for sizing circuit devices known in the art. The additional capacitance of keeper 212 may slow down circuit transitions due to additional capacitance introduced by keeper 212. Pull-down devices 204-210 may be unable to overcome keeper 212 during a time interval in which the inputs are expected to switch. To alleviate these detrimental effects on performance, keeper gating device 218 effectively disables keeper 212 during the time interval when the inputs are expected to switch. In most functional cases, inputs IN₀, IN₁,...IN_N switch during a known time interval within a clock cycle. Keeper 212 is disabled by keeper gating device 218 upon receipt of a high CONTROL signal at the gate input during a time when inputs IN₀, IN₁,...IN_N are expected to switch. Keeper gating device

218 then effectively enables keeper 212 when CONTROL transitions low, after the inputs IN_0, IN_1,...IN_N have completed switching.

[1018] In general, leakage currents slowly discharge a dynamic node. In circuit 200, the leakage current will not fully discharge dynamic node 216 or change the circuit output value unless keeper 212 is effectively disabled for a long period of time. Therefore, CONTROL is generally optimized to allow enough time for the circuit to evaluate correctly, while not keeping keeper 212 effectively disabled long enough for the leakage currents to change the value of dynamic node 216. The maximum time that keeper 212 can be effectively disabled, without compromising circuit evaluation, may be determined by simulation of the arrival time of inputs IN_0, IN_1,...IN_N for the particular circuit in a targeted manufacturing process, effectuating design rules that guarantee arrival times for IN_0, IN_1,...IN_N, or any other method for determining arrival times known in the art.

[1019] In FIG. 3, timing waveforms for CLOCK, inputs IN_1...IN_N, CONTROL, and dynamic node 216 illustrate the operation of circuit 200. At time t0, CLOCK is low and circuit 200 is in the precharge phase. Device 210 is disabled, device 202 is enabled, and node 216 is precharged high by device 202. Keeper 212 is on because OUT is low. Keeper gating device 218 is enabled because CONTROL is low. Thus, keeper 212 is effectively enabled and maintains the precharge on dynamic node 216. At time t1, CLOCK transitions high and circuit 200 enters the evaluation phase. Device 202 is disabled, device 210 is enabled, dynamic node 216 maintains a high value because keeper 212 remains effectively enabled by the low CONTROL signal.

[1020] The inputs, IN_0, IN_1,...IN_N do not begin to arrive until time t3. In one embodiment, devices 204-208 have the same size, gain, and sensitivity to keeper 212. These devices are sufficiently sized to overcome the precharge on dynamic node 216, but are not strong enough to overcome keeper 212. Keeper 212 is effectively disabled at t2 when CONTROL transitions high and disables keeper gating device 218. CONTROL transitions high before arrival of the fastest input to devices 204-208 to prevent keeper 212 from fighting a discharge of dynamic node 216 by devices 204-208. Between time t2 and t3, dynamic node 216 floats because the keeper path is

effectively disabled and neither a pull-down path to Vss nor the precharge path to VDD is enabled. At time t3, the fastest input arrives and at time t4, the slowest input arrives. After the slowest input arrives at t4, evaluation of dynamic node 216 completes. OUT switches according to the value of dynamic node 216, and configures keeper 212 consistent with the value of dynamic node 216. The effect of keeper 212 influences dynamic node 216 after CONTROL transitions to low at t5 and enables keeper gating device 218. Since, in this example, at least one of the input signals IN_0, IN_2,...IN_N is high during the interval between t4 and t6 of the evaluation phase, node 216 is discharged by the enabled transistors of devices 204-208 and OUT transitions high. When OUT transitions high, the gate of keeper 212 is high, keeper 212 is disabled, and dynamic node 216 remains discharged.

[1021] Circuit 200 enters the precharge phase again at time t6, after CLOCK transitions low. At time t7, circuit 200 enters the evaluation phase. CONTROL disables keeper 212 at time t8, before the arrival time of the fastest of signals IN_0, IN_1, ... IN_N. Since all of the inputs are low during this evaluation phase and keeper 212 is disabled, dynamic node 216 floats because a path from dynamic node 216 to either power or ground does not exist. However, since the time between t8 and t9 is sufficiently short to avoid leakage current from discharging dynamic node 216, circuit 200 evaluates properly to a low output value. The low value of OUT turns on keeper 212 and at time t9 when CONTROL turns on keeper gating device 218, keeper 212 is effectively enabled and properly reinforces the charge on dynamic node 216.

[1022] Dynamic node 216 may be susceptible to noise during the period between t8 and t9, where keeper gating device 218 effectively disables keeper 212 and dynamic node 216 is floating. In one embodiment, this noise may be counteracted by reducing the effective keeper strength instead of entirely disabling the keeper function. In some realizations, reduction in keeper strength is accomplished by including a weak keeper in addition to keeper 212 of circuit 200. This enhancement to circuit 200 is illustrated by circuit 400 in FIG. 4. Weak keeper 420 is always effective on dynamic node 216. Weak keeper 420 is a p-transistor that is minimally sized to properly overcome noise, but is not large enough to overcome leakage currents or to substantially impact evaluation or speed. The size of weak keeper 420 may be determined by simulating the circuit and setting the W/L ratio to achieve the

appropriate gain, or by any other method for sizing circuit devices known in the art. Although keeper 212 may be larger than prior art keeper devices, the impact of keeper 212 on the circuit performance is minimized by effectively disabling keeper 212 from dynamic node 216 while pull-down devices 204-208 are switching in response to inputs IN_0, IN_1,...IN_N.

[1023] The period when keeper 212 is disabled may vary depending upon the particular circuit characteristics. In one embodiment, keeper 212 is disabled long enough to allow the arrival of all input signals during the period where keeper 212 is disabled, but not long enough for leakage current to discharge dynamic node 216. CONTROL is designed to effectively disable keeper 212 before the fastest input arrives and to effectively enable keeper 212 after the slowest input arrives. The timing of CONTROL is determined by simulation or any other method for determining signal arrival times and leakage current discharge times.

[1024] In one embodiment, a subset of the pull-down devices is strong enough to overcome keeper 212 and keeper 212 is effectively disabled only during the arrival of the inputs to critical paths, i.e., paths including pull-down devices that are not strong enough to overcome keeper 212. CONTROL is designed to effectively disable keeper 212 before the fastest input arrives to a critical path and to effectively enable keeper 212 after the slowest input arrives to a critical path, but before leakage current discharges dynamic node 216.

[1025] In one embodiment, CONTROL is a pulse, based on CLOCK, and has a pulse-width corresponding to the period for effectively disabling keeper 212. In one embodiment, CONTROL is a self-timed signal, i.e., based on a delayed node, with a pulse-width corresponding to the period for effectively disabling keeper 212. The pulse circuitry may be implemented by any design technique known in the art.

[1026] The description of the invention set forth herein is illustrative, and is not intended to limit the scope of the invention as set forth in the following claims. For example, while a specific logic function has been described, the individual functionality may vary. The individual evaluation components are not critical to understanding the invention described herein and typically varies from circuit to circuit. The OR-type circuit of FIG. 2 is for illustration only, and other circuits (such

as NOR, NAND, AND, XOR, XNOR, etc.) may also benefit from the techniques described. Although the evaluation circuitry has been described as including n-channel devices and the keeper devices have been described as p-channel devices, the evaluation circuitry may include p-channel devices and the keeper devices may be n-channel devices. Moreover, the applications in which the invention may be applied are not limited to dynamic logic circuits, but may extend to other circuits with functions similar to the requirements of dynamic circuit. Other variations and modifications of the embodiments disclosed herein, may be made based on the description set forth herein, without departing from the scope and spirit of the invention as set forth in the following claims.